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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,372	10/09/2003	Dmitrii Yu Stepanov	50021-023	6384

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MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/681,372	STEPANOV ET AL.	
	Examiner	Art Unit	
	JASON E. MATTIS	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/19/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *17-19 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Response to Amendment filed 6/19/08. Due to the Amendment, the previous drawing objection has been withdrawn. Claims 17-19 and 21 have been withdrawn from consideration. Claims 1-21 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, 10, 12-14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al. (U.S. Pat. 6098176) in view of Tomsio et al. (U.S. Pat. 6737902 B2) and in further view of Arnett (U.S. Pat. 5909472).

With respect to claim 1, Coteus et al. discloses a distribution network for distributing a clock signal comprising a sequence of counter signals **(See the abstract of Coteus et al. for reference to a clock signal distribution network distributing a clock signal sequence to multiple electronic circuit devices)**. Coteus et al. also discloses a plurality of delivery points for facilitating simultaneous detection of a counter

signal to provide timing information **(See column 4 lines 37-59 and Figure 7 of Coteus et al. for reference to the system including multiple chips, which are delivery points, that detect different parts of a synchronous clock signal simultaneously)**. Coteus et al. further discloses the clock signal comprising a carrier whereby the sequence of counter signals is in the form of the carrier **(See column 3 lines 14-41 and Figures 2-4 of Coteus et al. for reference to clock signals comprising carriers used to detect the clock counts)**. Although Coteus et al. discloses simultaneously detect different parts of a clock signal, Coteus et al. does not specifically disclose simultaneous detection of different counter signals. Coteus et al. also does not specifically disclose the clock signal comprising a modulated carrier whereby a sequence of counter signals is in the form of an envelope of the carrier.

With respect to claim 20, Coteus et al. discloses a method of distributing a clock signal comprising a sequence of counter signals **(See the abstract of Coteus et al. for reference to a clock signal distribution network implementing a method to distribute a clock signal sequence to multiple electronic circuit devices)**. Coteus et al. also discloses providing the clock signal in the form of a carrier whereby the sequence of counter signals is in the form of the carrier **(See column 3 lines 14-41 and Figures 2-4 of Coteus et al. for reference to clock signals comprising carriers used to detect the clock counts)**. Coteus et al. further discloses simultaneously detecting a counter signal at a plurality of delivery points to provide timing information **(See column 4 lines 37-59 and Figure 7 of Coteus et al. for reference to the system including multiple chips, which are delivery points, that detect different parts of a**

synchronous clock signal simultaneously). Although Coteus et al. discloses simultaneously detect different parts of a clock signal, Coteus et al. does not specifically disclose simultaneous detection of different counter signals. Coteus et al. also does not specifically disclose the clock signal comprising a modulated carrier whereby a sequence of counter signals is in the form of an envelope of the carrier.

With respect to claim 12, Coteus et al. does not disclose a clock signal being multiplexed into a plurality of channels comprising two or more sequences of counter signals in different channels.

With respect to claims 13 and 14, Coteus et al. does not disclose varying the spatial pitch and time delays of the different clock signal channels to provide different groups of delivery points.

With respect to claims 1, 12-14, and 20, Tomsio et al., in the field of communications, discloses a clock signal being multiplexed into a plurality of channels comprising two or more sequences of counter signals in different channels with the sequences being varied in spatial pitch or in time delay **(See column 2 lines 22-61 of Tomsio et al. for reference to using multiple clock signals being detected at the same time and having either different delays or different lengths, which correspond to different spatial pitches)**. Using a clock signal being multiplexed into a plurality of channels comprising two or more sequences of counter signals in different channels with the sequences being varied in spatial pitch or in time delay has the advantage of allowing multiple clock paths to be used such that it is easier for more devices to use the clock signal.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Tomsio et al., to combine using a clock signal being multiplexed into a plurality of channels comprising two or more sequences of counter signals in different channels with the sequences being varied in spatial pitch or in time delay, as suggested by Tomsio et al., with the system and method of Coteus et al., with the motivation being to allow multiple clock paths to be used such that it is easier for more devices to use the clock signal.

With respect to claim 10, Coteus et al. does not specifically disclose the clock signal comprising an amplitude, phase, or frequency modulated carrier.

With respect to claims 1, 10, and 20, Arnett, in the field of communications, discloses a clock signal comprising a frequency modulated carrier whereby a sequence of counter signals of the clock signal is in the form of an envelope of the carrier **(See the abstract, column 2 lines 4-31, and column 3 line 24 to column 4 line 5 of Arnett for reference to a clock signal being in the form of a frequency modulated carrier where the envelope of the carrier is used to detect the clock signal)**. Using a clock signal comprising a frequency modulated carrier has the advantage of reducing EMI interference **(See column 1 lines 42-44 of Arnett for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Arnett, to combine using a clock signal comprising a frequency modulated carrier, with the system and method of Coteus et al. and Tomsio et al., with the motivation being to reduce EMI interference.

With respect to claim 2, Coteus et al. discloses that path length difference between delivery points are chosen to be equal to or a multiple of a spatial pitch of the sequence of counter signals **(See column 4 lines 48-59 and Figure 7 of Coteus et al. for reference to choosing line lengths between delivery points to be equal to or multiples of a half wavelength at the clock frequency, which is a spatial pitch of the clock signal)**.

With respect to claim 3, Coteus et al. discloses the network being a star network **(See column 4 lines 48-59 and Figure 7 of Coteus et al. for reference to the network being a star-type network with one source and multiple spokes receiving the clock signal from the source)**.

With respect to claims 4, 6, and 7, Coteus et al. discloses the clock signal network comprising a resonant structure coupled via nodes that is arranged to generate and maintain the clock signal **(See column 2 line 38 to column 3 line 13 of Coteus et al. for reference to using resonant transmission lines between chip devices that are nodes to form a resonant network structure to generate and maintain the clock signal distribution)**.

With respect to claim 5, Coteus et al. discloses an external clock source coupled into the resonant structure **(See column 4 lines 48-59 and Figure 7 of Coteus et al. for reference to for reference to an external clock source 52 being coupled into the resonant network structure)**.

With respect to claim 9, Coteus et al. discloses the network comprising a plurality of intersecting sub-networks **(See column 4 lines 60-64 and Figure 8 of**

Coteus et al. for reference to the network having branches to multiple sub-networks).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 11, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al. in view of Tomsio et al. and Arnett, and in further view of Iida et al. (U.S. Pat. 6108465).

With respect to claim 8, the combination of Coteus et al., Tomsio et al., and Arnett does not disclose the resonant structure being a ring.

With respect to claim 11, the combination of Coteus et al., Tomsio et al., and Arnett does not disclose the clock signal being an optical clock signal.

With respect to claims 8 and 11, Iida et al., in the field of communications, discloses an optical clock signal used to distribute timing information in a resonant ring network **(See column 1 lines 34-52 of Iida et al. for reference to distributing an optical clock signal in a resonant ring network)**. Using an optical clock signal used

to distribute timing information in a resonant ring network has the advantage of allowing high speed optical transmission to transmit clock information at a higher frequency.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Iida et al., to combine using an optical clock signal used to distribute timing information in a resonant ring network, as suggested by Iida et al., with the system and method of Coteus et al. Tomsio et al. and Arnett, with the motivation being to allow high speed optical transmission to transmit clock information at a higher frequency.

With respect to claims 15 and 16, the combination of Coteus et al., Tomsio et al., and Arnett does not disclose a WDM multiplexed optical clock signal.

With respect to claims 15 and 16, Iida et al. discloses using a WDM multiplexed optical clock signal **(See column 1 lines 34-52 of Iida et al. for reference to using multiplexed multiple clock signals having different frequencies, meaning the must also have different wavelengths)**. Using a WDM multiplexed optical clock signal has the advantage of allowing multiple clock signals to be sent on the same line at the same time.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Iida et al., to combine using a WDM multiplexed optical clock signal, as suggested by Iida et al., with the system and method of Coteus et al., Tomsio et al., and Arnett, with the motivation being to allow multiple clock signals to be sent on the same line at the same time.

Response to Arguments

6. Applicant's arguments with respect to claims 1-16 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON E. MATTIS whose telephone number is (571)272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571)272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason E Mattis
Examiner
Art Unit 2616

JEM
/Jason E Mattis/
Examiner, Art Unit 2616